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APPLICATION FOR UNITED STATES LETTERS PATENT

INVENTOR: Robert BAUER
Werner ERTLE
Till FROHNMÜLLER
Bernd GOLLER
Reinhard GREIDERER
Oliver NAGLER
Olaf SCHMECKEBIER
Wolfgang STADLER

TITLE: INTEGRATED SEMICONDUCTOR STRUCTURE

ATTORNEY: Anthony P. Curtis, Ph.D.
Reg. No. 46,193
BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

Description

Integrated semiconductor structure

The invention relates to an integrated semiconductor structure, having a substrate, at least one semiconductor element located on the substrate, a pad metal having a surface, a multiplicity of metal layers which are located between the pad metal and the substrate, and a multiplicity of insulation layers, which separate the metal layers from one another, the pad metal extending at least over part of the at least one semiconductor element.

A semiconductor structure of this type is known, for example, from US 6,207,547.

An important aspect in the fabrication of integrated semiconductor structures is the electrical contacting (bonding) of the semiconductor elements which are located within the semiconductor structure. In this case, the electrical contact between housing contacts (PINs) and the semiconductor elements is produced via contact islands. The contact islands are metallic regions (pad metal) which can be electrically connected to the semiconductor elements and metal layers. On account of the bonding processes which are currently used, the pad metals are of a relatively large size in the semiconductor structure compared to the dimensions of the semiconductor elements below. The pad metal therefore covers a significant part of the surface of a chip, and consequently the region which lies below the pad metal forms a significant proportion of the volume of the chip.

During bonding of the semiconductor structure, a high mechanical load is exerted on the pad metal. This load brings with it the risk of structures disposed beneath the pad metal being damaged. For example, the top

insulation layer, which runs directly beneath the pad metal, may become cracked, leading to leakage currents on account of the passivation of the semiconductor structure being damaged. Secondly, the semiconductor elements, for example active structures, such as MOS transistors, which have a relatively thin gate oxide, must under all circumstances be protected from excessive pressure for reasons of reliability. Therefore, previously semiconductor elements have not been positioned beneath the pad metal, in order to avoid damage. This means that an extremely large loss of chip area has to be accepted.

EP 1 017 098 A2 proposes a combination of a stress-absorbing metal layer and a mechanically reinforced electrical insulation layer, as well as a sufficient thickness of these two layers, so that at least part of the semiconductor element may extend directly beneath the pad metal. However, this only slightly reduces the area taken up on the chip surface.

It is known from US 6,207,547, which was mentioned in the introduction, to introduce a structured intermediate layer between pad metal and top metal level in order to stabilize and protect the active circuits below. The result of this is that structures with gate oxide, for example MOS transistors, can be positioned directly below the pad metal. However, the production of a structured intermediate layer of this type requires a specially modified and complicated production process.

Therefore, it is an object of the present invention to propose a semiconductor structure which allows a simplified production process to be used without there being any restriction with regard to the use of semiconductor elements which may be positioned beneath the pad metal.

According to the invention, the object is achieved by an integrated semiconductor structure of the type described in the introduction in which, below the surface of the pad metal, at least the top two metal layers have a structure which in each case at least includes two adjacent interconnects.

The invention is based on the discovery that a damping and stabilizing structure can be formed by using a suitable arrangement (layout) of the top two metal levels lying directly beneath the pad metal without the fabrication process for the integrated semiconductor structure having to be altered. Furthermore, the inventors have discovered that on account of the increased stability of this semiconductor structure any type of semiconductor element can be arranged beneath the surface of the pad metal.

Contrary to designs which have long been known, the interconnects of the present invention can be electrically utilized and are not used just to increase stability. For example, the interconnects running beneath the pad metal are connected to one or different potentials on the semiconductor structure. The interconnects of the top metal layer are typically used as supply lines for semiconductor elements (e.g. transistors) below.

Depending on the technology used, the number of metal layers may be between 3 and 11, for example between 4 and 8 metal layers are currently used for the 0.13 µm CMOS technology generation.

A configuration of the integrated semiconductor structure according to the invention provides for the number of interconnects, within a metal layer, at least below the surface of the pad metal, to be between 2 and 6, depending on the size and extent of this pad metal.

According to the invention, the interconnects within a metal layer may be electrically insulated from one another.

In a further development, the interconnects within a metal layer are electrically connected to one another. Furthermore, if there are more than two interconnects below the surface of the pad metal, individual interconnects within a metal layer can be electrically insulated from the other interconnects, the remaining interconnects being electrically connected to one another.

It is also conceivable for structures, known as dummy structures, which have purely a stabilizing function but are not electrically connected to any potential, to be incorporated at least in small regions below the surface of the pad metal. However, this design leads to a loss of electrically usable area.

A further advantageous configuration which shields the structures located beneath the pad metal from the mechanical load provides for the interconnects to be designed to be sufficiently wide and to be at relaxed spacings from one another. According to the invention, the ratio between the width of the interconnects and the spacing between them is between 3 and 20, preferably 10. At least the top two metal layers are therefore designed as wide interconnects in order to achieve a damping effect without requiring any unnecessary procedures.

In a particularly advantageous further development of the integrated semiconductor structure according to the invention, at least below the surface of the pad metal there is a multiplicity of vias which electrically connect the interconnects of the top metal layer to the interconnects of the metal layer below, the vias penetrating vertically through the insulation layer

between the top two metal layers. This firstly ensures that the semiconductor element still functions even in the event of a short circuit occurring between these metal layers, as may occur as a result of mechanical pressure. Secondly, the vias further stabilize the integrated semiconductor structure.

Optimized stabilizing and damping can be achieved by suitable formation of the vias. It is preferable for a relatively large number of vias between the top two metal layers to be distributed beneath the surface of the pad metal, the vias being arranged in series with one another or offset with respect to one another. In this way, any pressure which occurs is distributed over the largest possible area.

Another advantageous development of the integrated semiconductor structure according to the invention provides for the interconnects of the top two metal layers to have a multiplicity of apertures at least below the surface of the pad metal. These apertures may be filled with the same material as the material which forms the insulation layers, such as for example silicon dioxide or silicon nitride. This too additionally stabilizes the semiconductor structure.

In another further development of the integrated semiconductor structure according to the invention, the apertures, at least below the surface of the pad metal, have a total area of between 5% and 30% of the total area of the interconnects. The apertures preferably form 20% of the interconnects.

According to the invention, the stability of the integrated semiconductor structure with respect to pressures which occur is also increased by the interconnects of the top two metal layers being arranged in such a manner with respect to one another that the apertures in the top interconnects are offset

with respect to the apertures in the interconnects below. This offset arrangement ensures a high degree of damping.

In another embodiment of the integrated semiconductor structure according to the invention, the interconnects of the top metal layer lie approximately congruently above the interconnects of the metal layer below.

The interconnects of the top metal layer are preferably offset with respect to the interconnects of the metal layer below. This results in a very effective damping structure being formed. The lateral offset between the interconnects may in this case be at its maximum, in which case therefore two adjacent interconnects of a metal layer are partially covered by, for example, the interconnect above.

A further advantageous configuration of the integrated semiconductor structure provides for the metal layers, at least for the most part, to be made from a sufficiently hard metal. This makes it possible to prevent the thickness of the metal layers from being reduced under mechanical load or to prevent the insulation layer located above the metal layer from being pushed through to the insulation layer below under mechanical load.

The metal is typically copper, aluminum, tungsten, molybdenum, silver, gold, platinum or alloys thereof.

In another refinement, the surface of the pad metal covers a region which, within a metal layer, comprises at least 50% metal. These preferably include the metallic regions of the interconnects (without apertures), but also additionaly introduced metallic dummy structures.

For a particularly stable configuration of the integrated semiconductor structure, the metal is distributed uniformly below the surface of the pad metal. Therefore, the interconnects which consist of metal and the apertures within the interconnects and also the electrical connection between adjacent interconnects are preferably distributed uniformly beneath the surface of the pad metal.

There is preferably a top insulation layer between the pad metal and the top metal layer, the top insulation layer having a first thickness D1 and the top metal layer having a second thickness D2, and the ratio between the two thicknesses D1 and D2 being between 1 and 5. This reduces the risk of cracks forming in the top insulation layer and therefore provides increased protection for the semiconductor elements below.

Another development of the integrated semiconductor structure according to the invention provides for the top insulation layer to have a thickness D1 and for the pad metal to have a thickness D3, and for the ratio between the two thicknesses D1 and D3 to be between 0.5 and 3.

The invention is described in more detail below with reference to the figures, in which:

Fig. 1 shows a cross section through an exemplary embodiment of an integrated semiconductor structure according to the invention,

Fig. 2 shows part of the interconnects of the top two metal layers from figure 1, in a perspective illustration,

Fig. 3 shows a plan view of an integrated semiconductor structure according to the invention with a pad metal and interconnects.

The semiconductor structure includes a pad metal 3 having a surface F and a thickness D3, for example a thick layer of aluminum, a passivation 8, a substrate 1, a semiconductor element 2, for example a transistor 2, positioned on the substrate, the transistor 2 being arranged beneath the surface F of the pad metal 3, a multiplicity of metal layers 4.x, and a multiplicity of insulation layers 5.y which separate the metal layers 4.x from one another. For the sake of clarity, fig. 1 diagrammatically depicts only the first and top two metal layers 4.1, 4.x-1 and 4.x; depending on the technology used, currently up to 11 metal layers 4.x may be arranged above one another.

To form a shield with respect to the mechanical pressure which is produced bonding or testing of the integrated semiconductor structure, both the pad metal 3 and the top insulation layer 5.y, which is located directly beneath the pad metal 3, are designed to be sufficiently thick. The insulation layer 5.y preferably has a thickness D1 which is between one and five times as thick as the thickness D2 of the top metal layer 4.x and is between 0.5 and three times as thick as the thickness D3 of the pad metal 3.

The top two metal layers 4.x and 4.x-1 are separated from one another by an insulation layer 5.y-1. The vias 6 penetrate vertically through this insulation layer 5.y-1 and electrically connect the top metal layer 4.x to the metal layer 4.x-1 below. Particularly in the region below the surface F of the pad metal 3 there is a multiplicity of vias 6 between the two metal layers 4.x and 4.x-1. These configurations provide sufficient protection for the transistor 2 with respect to mechanical loads which occur.

Figure 2 shows a perspective illustration of part of the integrated semiconductor structure according to the

invention in the region of the top two metal layers directly below the surface of the pad metal. Both the interconnect 4.x.z of the top metal layer and the interconnect 4.x-1.z of the metal layer below have apertures 7.x and 7.x-1. The apertures 7.x in the interconnects 4.x.z are arranged offset with respect to the apertures 7.x-1 of the interconnect 4.x-1.z below. The apertures 7.x and 7.x-1 therefore do not lie directly above one another. Furthermore, the two interconnects 4.x.z and 4.x-1.z are electrically connected to one another via vertically running vias 6. To ensure the maximum possible stability with respect to pressures, as many vias 6 as possible are arranged in particular in the region beneath the pad metal.

Other arrangement of apertures 7.x and vias 6 will result when the person skilled in the art applies his specialist knowledge and abilities.

Figure 3 shows a plan view of the integrated semiconductor structure according to the invention with a pad metal 3 and an adjoining pad metal 3. Four interconnects 4.x.1 to 4.x.4 run in the region beneath the pad metals 3. The fifth interconnect 4.x.5 runs outside the region of the pad metals 3. The spacings A between the individual interconnects 4.x.z and their width B are clearly shown. Semiconductor elements, such as transistors or diodes, likewise lie beneath the surface of the pad metal 3 but are not visible in figure 3.

The overall result of the invention is that a suitable damping and stabilizing structure which enables any type of electrical semiconductor elements to be arranged beneath the surface of the pad metal without there being any risk of damage to these semiconductor elements in the event of pressures, as occur, for example, during bonding or testing, is achieved even without expensive process changes or without the need

for additional process features to be added. Furthermore, it is now possible to utilize the region beneath the surface of the pad metal, for example for power supply tracks.